

Structure Silicon monolithic integrated circuit
 Product Name Camera Image Adaptive Enhancer IC for security devices

Type **BU1570KN**

- Function
- Compatible with image data up to UXGA size (1600x1200) 7.5 fps, SXGA size (1280x1024)15 fps, and VGA size (640x480) 30 fps.
 - In/Output data format is compatible with YUV=4:2:2 8bit. Order of components may be adjusted by the register.
 - Operation modes are image enhance mode, through mode, and sleep mode.
 - Strength of image correction can be set to linear.
 - Able to read out brightness for the entire area for movement detection
 - Register can be set up with a 2-line serial interface.
 - Compatible with 2 power sources (VDDIO=3.3V:TYP, VDD=1.50V:TYP).

○ Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Applied power source voltage1(IO)	VDDIO	-0.3~+4.2	V
Applied power source voltage2(CORE)	VDD	-0.3~+2.1	V
Power dissipation	PD	450*1, 690*2	mW
Input voltage	VIN	-0.3~VDDIO+0.3	V
Storage temperature range	Tstg	-40~+125	°C
Operating temperature range	Ta	-40~+85	°C

*1 IC only. In the case exceeding 25°C, 4.5mW should be reduced at the rating 1°C.

*2 When packaging a glass epoxy board of 70x70x1.6mm. If exceeding 25°C, 6.9mW should be reduced at the rating 1°C.

* Has not been designed to withstand radiation.

* Operation is not guaranteed.

○ Operating conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Applied power source voltage1(IO)	VDDIO	2.70	3.30	3.60	V
Applied power source voltage 2(CORE)	VDD	1.45	1.50	1.55	V
Input voltage range	VIN-VDDIO	0	-	VDDIO	V

* Please supply power source in order of VDD→VDDIO.

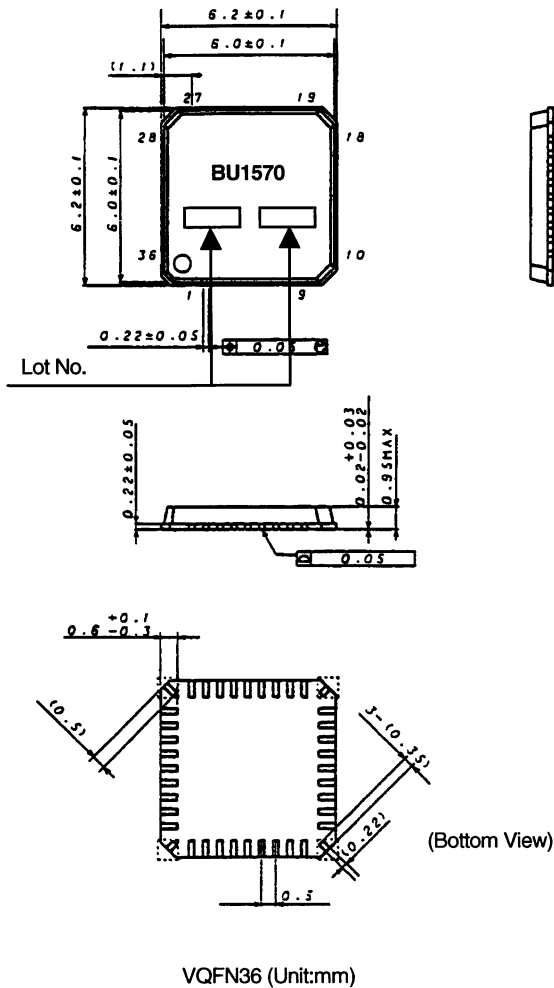
Status of this document

The Japanese version of this document is the formal specification. A customer may use this translation version only for a reference to help reading the formal version. If there are any differences in translation version of this document, formal version takes priority.

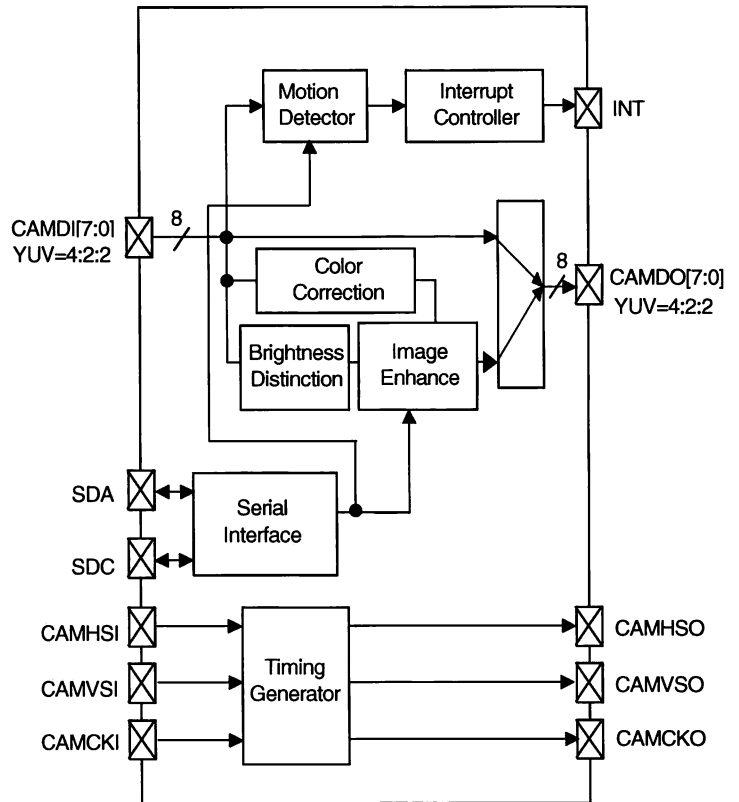
○ Electric Characteristics (Unless otherwise specified, VDD=1.50V, VDDIO=3.30V, GND=0.0V, Ta=25°C, f_{IN}=52.0MHz)

Parameter	Symbol	Limits			Unit	Condition
		MIN.	TYP.	MAX.		
Input frequency	f _{IN}	10.0	-	52.0	MHz	CAMCKI(DUTY45%~55%)
Static consumption current	IDDst	-	-	30	μA	At sleep mode setting, input terminal = GND setting
Input "H" current 1	I _{IH1}	-10	-	10	μA	V _{IH} =VDDIO
Input "H" current 2	I _{IH2}	35	70	140	μA	Pull-Down terminal, V _{IH} =VDDIO
Input "L" current 1	I _{IL1}	-10	-	10	μA	V _{IL} =GND
Input "L" current 2	I _{IL2}	-10	-	10	μA	Pull-Down terminal, V _{IL} =GND
Input "H" voltage 1	V _{IH1}	VDDIO x 0.8	-	VDDIO +0.3	V	Normal input (including input mode of I/O terminal)
Input "L" voltage 1	V _{IL1}	-0.3	-	VDDIO x 0.2	V	Normal input (including input mode of I/O terminal)
Input "H" voltage 2	V _{IH2}	VDDIO x 0.85	-	VDDIO +0.3	V	Hysteresis input (RESETB, CAMCKI, SDA, SDC)
Input "L" voltage 2	V _{IL2}	-0.3	-	VDDIO x 0.15	V	Hysteresis input (RESETB, CAMCKI, SDA, SDC)
Output "H" voltage	V _{OH}	VDDIO -0.4	-	VDDIO	V	I _{OH} =-1.0mA(DC) (including input mode of I/O terminal)
Output "L" voltage	V _{OL}	0.0	-	0.4	V	I _{OL} =1.0mA(DC) (including input mode of I/O terminal)

○ External Dimensional Drawing and Mark Drawing



○ Block Diagram



○ Terminal Functions

Pin No.	Pin name	Function Explanation
1	CAMVSI	Vertical Timing Input
2	N.C.	
3	CAMHSI	Horizontal Timing Input
4	CAMD10	Data Input Bit 0
5	CAMD11	Data Input Bit 1
6	CAMD12	Data Input Bit 2
7	CAMD13	Data Input Bit 3
8	CAMD14	Data Input Bit 4
9	CAMD15	Data Input Bit 5
10	CAMD16	Data Input Bit 6
11	CAMD17	Data Input Bit 7
12	VDDIO	DIGITAL IO Power Source
13	CAMCKI	Clock Input
14	GND	Common GROUND
15	VDD	CORE Power Source
16	SDA	In/Output Serial Data
17	SDC	In/Output Serial Clock
18	INT	Brightness Change Interruption Signal
19	CAMVSO	Vertical Timing Signal Output
20	N.C.	
21	CAMHSO	Horizontal Timing Signal Output
22	CAMDO0	Data Output: Bit 0
23	CAMDO1	Data Output: Bit 1
24	CAMDO2	Data Output: Bit 2
25	CAMDO3	Data Output: Bit 3
26	CAMDO4	Data Output: Bit 4
27	CAMDO5	Data Output: Bit 5
28	CAMDO6	Data Output: Bit 6
29	CAMDO7	Data Output: Bit 7
30	TEST1	Test Mode Terminal 1 (Connect to GND)
31	TEST2	Test Mode Terminal 2 (Connect to GND)
32	RESETB	System Reset Signal
33	VDDIO	DIGITAL IO Power Source
34	CAMCKO	Clock Output
35	GND	Common GROUND
36	VDD	CORE Power Source

○ Cautions on use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.

In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.

Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern

If small-signal GND and large-current GND are provided, it will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

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